Gregory Ichneumon Brown
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I am looking to combine my 10 years of engineering experience with my new skills in machine learning and data mining. I have expertise in:

- Designing, building, and maintaining complex software systems.
- Natural Language Processing, Data Mining of information, and Machine Learning.
- Optimizing software and hardware in multiprocessor and distributed environments**.**

Education

University of Colorado at Boulder, MS Computer Science **Exp. Graduation: May 2011**
Selected classes: Machine Learning, Natural Language Processing, *Current GPA: 3.96*
Multi-Robot Systems, Chaotic Dynamics, Networking Systems, Information Retrieval, Data Mining

Cornell University, BS Electrical Engineering **Graduated May 2000**

Recent Research Projects

Master's Thesis: Relation Extraction on the JDPA Sentiment Corpus **August 2010 - Present**
Using the JDPA Sentiment Corpus to learn to recognize relationships between entities expressed in an English language blog document.

- Relations between mentions across multiple sentences classified using Support Vector Machines.
- Binary Feature Vectors and Tree Kernels.
- Ensemble prediction of entity relations from relations between mentions.

Accelerating System Performance Profiling with Machine Learning **Sept 2009-July 2010**
Learn from an expert human's analysis of a computer system's performance metrics which metrics are most likely to lead to the root cause of performance anomalies.

- Investingated the use of Support Vector Machines, Random Forests, and other Ensemble machine learning techniques using libSVM and Weka.
- Time series analysis using non-linear dynamic systems techniques

Genetic Algorithm/Programming Research **Feb 2008-July 2008**
Personal programming and research project which led me to go to grad school.

- Used ECJ open source Java based evolutionary computation platform to research a self adaptive genetic programming method.

Technical Skills/Technologies

Machine Learning Methods Used: Support Vector Machines, Ensemble Learning, Hidden Markov Models, Conditional Random Fields, Topic Modelling, Robust Risk Minimization, Bayesian Modeling

ML/NLP Tools: Lexical Parser for tokenization (JFlex), Weka Machine Learning System, libSVM, libLinear, SVMLight, SVMLight-TK, CRF++, YamCha, Stanford Parser, Lucene, Mallet

Development Experience: Networking and distributed Systems, Multiprocessor Systems, Embedded Systems; Hardware design and verification; Object-Oriented Programming; Multi-threading; Processor and memory system performance analysis; Lab verification and debug; UML diagrams

Languages: Java, Scala, C, C++, Perl, Python, MIPS Assembly, Verilog, Vera, Matlab, VB, Unix scripting, Ant, SystemC, R, LISP, SQL, HTML/CSS, PHP

Technologies/Tools: TCP/IP, pthread, XML; MIPS Processors, DDR1/2/3 SDRAM Memory Systems; H.264 Video; High Definition Video; PCI; PowerPC Processors; FPGAs; Amazon Web Services; gcc; make; CVS; Subversion; Git; Eclipse; Microsoft Visual Studio; MySQL; VCS; LEDA; Covermeter; Clearcase; Clearquest; Xilinx ISE; Excel; Hspice; Oscilloscopes; Logic Analyzers; GPIB control of instruments; Signal Generators.

Employment History

JD Power and Associates: Web Intelligence **May 2010-Dec 2010**
Research Internship on blog sentiment analysis research team. *Boulder, CO*

- Designed and built an integrated research environment in Scala/Java to allow the science team to quickly develop and improve sentiment analysis algorithms.
- System includes: text tokenization, part-of-speech tagger, dependency parser, support for multiple machine learning methods, datastructures for efficient document and sentiment representation and manipulation, modular system for loading/saving text files in different file formats including XML and CoNLL.
- Created improvements to rule based tokenization system.
- Researched IOB sequence labeling of sentiment expressions and entity mentions using conditional random fields and greedy robust risk minimization.
- Created UML diagrams of system.
- Created build scripts (ant and Eclipse) and organized project structure.
- Optimized sentiment representation data structructures for fast (sub-linear) access time.

Missing Link Consultants **Dec 2007-Apr 2008**
Independent website software contractor. *Christchurch, New Zealand*

- Created Drupal/PHP based website for local business.

Broadcom Corporation **May 2005-July 2007**
Hardware Verification Engineer in Consumer Electronics Group *Andover, MA*
System-on-a-Chip High Definition Video Chip BCM7043 and Blu-Ray Chip: BCM7440
H.264 Video Encoding/Decoding with DDR SDRAM, multiple MIPS/ARC processors.

- Creating a multi-threaded C++ verification environment for running directed and randomized testing a the memory system.
- Verified transaction cache coherency, correct handling of cache line fills, and correct handling of all transaction types for MIPS OCP bridge bus.
- Debugged Perl compilation scripts for distributed, simultaneous hardware simulations.
- Tailored MIPS bootloader in assembly to work in custom verification environment.
- Wrote raw video preprocessing algorithms in C.
- Improved Microsoft Visual Studio based C++ verification platform.
- Verified H.264 video encoder.
- Improved C TCP socket between host PC and Unix hardware simulation.
- Planned and executed verification plans for multiple parts of the system.

Teradyne Incorporated, Semiconductor Test Division **June 2000-April 2005**
Hardware Design Engineer in System Platform Group for FLEX tester *Boston, MA*

- Developed distributed Digital Signal Processing Subsystem.
- Designed and implemented custom FPGA Router with DDR SDRAM buffering memory.
- Technical lead for router project starting in early 2002 and coordinated work with other engineers to close timing and complete verification.
- Created Vera/Perl distributed testing environment.
- Performed memory system performance analysis and made improvements to system.
- Verified DSP subsystem consisting of FPGA router, 4 PowerPC custom processing modules running VXWorks RTOS, and a host PC. Found and resolved intermittent software and hardware bugs caused by intricate interactions in the system.
- Led investigation of performance improvements: G5 PowerPC processor, 10 Gigabit Ethernet
- Coordinated design of Low Jitter Clock Instrument Design: Picoclock
- Spice simulation, Schematic entry, board layout, and lab debug of systems

Publications

G I Brown, "An Examination of the Local Dynamics of Computer Performance," in Projects in Chaotic Dynamics, University of Colorado Department of Computer Science, Technical Report CU-CS 1060-10 (www.cs.colorado.edu/publications), 2010.

US Patent #6966019: Instrument Initiated Communication for ATE (Teradyne), 2002